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electrical contacts at the opposite edges of the substrate configured to allow communications through the channels via the electrical contacts.

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4 2. An apparatus as recited in claim 1 wherein the substrate has a first
5 side and a second side, the plurality of memory devices being disposed on both
6 sides of the substrate.

7
8 3. An apparatus as recited in claim 1 wherein the substrate has a first
9 side and a second side, the plurality of channels extending across both sides of the
10 substrate.

11
12 4. An apparatus as recited in claim 1 wherein each channel includes a
13 plurality of conductors, the plurality of conductors following a substantially linear
14 path across the substrate.

15
16 5. An apparatus as recited in claim 1 wherein each channel includes a
17 plurality of conductors, the plurality of conductors having lengths that are
18 approximately equal.

19
20 6. (Amended) An apparatus as recited in claim 1 wherein the substrate
21 has one or more surfaces and the memory devices are mounted on such one or
22 more surfaces of the substrate.

23
24 7. (Amended) An apparatus comprising:
25

1 a first substrate having a plurality of memory devices disposed thereon and
2 a first channel portion extending across the first substrate, the first substrate
3 having opposite ends and contacts at the opposite ends to allow communications
4 through the first channel portion via the contacts at the opposite ends of the first
5 substrate;

6 a second substrate having a plurality of memory devices disposed thereon
7 and a second channel portion extending across the second substrate, the second
8 substrate having opposite ends and contacts at the opposite ends to allow
9 communications through the second channel portion via the contacts at the
10 opposite ends of the second substrate; and

11 a first connector configured to communicatively couple the first channel
12 portion to the second channel portion through at least some of the contacts of the
13 first and second substrates, wherein the first connector engages contacts at a first
14 of the ends of the first substrate and engages contacts at a first of the ends of the
15 second substrate;

16
17 **8.** An apparatus as recited in claim 7 wherein the coupling of the first
18 channel portion to the second channel portion through the connector forms a
19 channel.

20
21 **11.** An apparatus as recited in claim 7 wherein the first channel portion
22 includes a plurality of conductors following a substantially linear path across the
23 first substrate.
24
25

1 **12.** An apparatus as recited in claim 7 wherein the second channel
2 portion includes a plurality of conductors following a substantially linear path
3 across the second substrate.

4
5 **13.** An apparatus as recited in claim 7 wherein the first channel portion
6 includes a plurality of conductors having lengths that are approximately equal.

7
8 **14.** An apparatus as recited in claim 7 wherein the second channel
9 portion includes a plurality of conductors having lengths that are approximately
10 equal.

11
12 **15.** An apparatus as recited in claim 7 further including a third substrate
13 coupled to the first connector.

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15 **16.** An apparatus as recited in claim 15 wherein the third substrate
16 includes a third channel portion extending across the third substrate.

17
18 **17.** An apparatus as recited in claim 15 wherein the third substrate
19 includes a third channel portion extending across the third substrate, the third
20 channel portion including a plurality of conductors following a substantially linear
21 path across the third substrate.

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23 **18.** An apparatus as recited in claim 15 wherein the third substrate
24 includes a third channel portion extending across the third substrate, the third
25

1 channel portion including a plurality of conductors having lengths that are
2 approximately equal.

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4 **19. (Amended)** An apparatus as recited in claim 7 further including a
5 second connector that engages contacts at a second of the ends of the first
6 substrate and engages contacts at a second of the ends of the second substrate.

7
8 **20.** An apparatus as recited in claim 19 wherein the second connector is
9 coupled to a motherboard.

10
11 **21. (Amended)** An apparatus comprising:
12 a motherboard; and
13 a first memory module having contacts at opposite ends thereof, a first
14 channel portion extending across the first memory module between the contacts;
15 a second memory module having contacts at opposite ends thereof, a
16 second channel portion extending across the second memory module between the
17 contacts;
18 a first connector coupling the first memory module to the second memory
19 module through contacts at first ends of the first and second memory modules; and
20 a second connector that engages contacts at the second ends of the first and
21 second memory modules.

22
23 **23.** An apparatus as recited in claim 21 wherein a channel extends
24 across the first memory module, the second memory module, and the first
25 connector.

2 **24. (Amended)** A method comprising:

3 arranging channel portions on a substrate such that the channel portions
4 extend between opposite edges of the substrate;

5 arranging contacts at the opposite edges of the substrate to allow
6 communication through the channel portions;

7 arranging channel portion conductors such that the length of the channel
8 portion conductors between opposite edges of the substrate is approximately
9 equal; and

10 coupling together a pair of such substrates using a connector, a channel
11 extending across the pair of substrates and the connector.

12
13 **25.** A method as recited in claim 24 further including propagating
14 signals through the channel.

15
16 **26.** A method as recited in claim 24 further including arranging a
17 plurality of memory devices on the substrate such that each memory device is
18 coupled to a channel portion.

19
20 **27.** A method as recited in claim 26 further including propagating
21 signals through the channel portions to perform memory operations.

22
23 **28.** A method as recited in claim 24 wherein each channel portion
24 includes a plurality of conductors, each of the conductors having approximately
25 equal lengths along the entire length of the channel portion.

1
2 **29.** A method as recited in claim 24 wherein each channel portion
3 includes a plurality of conductors following a substantially linear path across the
4 substrate.
5

6 **30.** A method as recited in claim 24 wherein channel portions are
7 arranged on both sides of the substrate.
8

9 **31. (New)** A memory system comprising:
10 first and second memory modules;
11 each of the first and second memory modules having contacts at first and
12 second opposite ends thereof and having one or more communication channel
13 portions extending between the contacts;
14

15 each of the first and second memory modules having a surface and one or
16 more memory devices mounted to the surface, the one or more memory devices
17 being communicatively coupled to the one or more communication channel
18 portions;
19

20 one or more board connectors that engage the contacts at the first ends of
21 the first and second memory modules to allow communications through the one or
22 more communication channel portions of the memory modules;
23

24 a coupling that engages the contacts at the second ends of the first and
25 second memory modules, the coupling being configured to communicatively
couple the one or more channel portions of the first and second memory modules
and to thereby form one or more communication channels that each comprise at

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1 least one of the communication channel portions of the first memory module and
2 at least one of the communication channel portions of the second memory module.

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4 **32. (New)** A memory system as recited in claim 31, wherein the
5 communication channel portions comprises a plurality of conductors following
6 substantially linear paths across the respective memory modules.

7
8 **33. (New)** A memory system as recited in claim 31, wherein each
9 communication channel portion comprises a plurality of conductors having lengths
10 that are approximately equal.

11
12 **34. (New)** A memory module comprising:
13 a substrate having opposite ends and at least one surface;
14 contacts at the opposite ends of the substrate;
15 one or more memory devices mounted to the surface of the substrate; and
16 one or more communication channel portions extending across the module
17 between the contacts, the one or more communication channel portions being
18 configured to allow communications through the contacts with the one or more
19 memory devices.

20
21 **35. (New)** A memory module as recited in claim 34, wherein the
22 substrate has opposing surfaces, and the one or more memory devices comprise at
23 least one memory device mounted on each of the opposing surfaces of the
24 substrate.
25

1 **36. (New)** A memory module as recited in claim 34, wherein the
2 substrate has opposing surfaces, and the one or more communication channel
3 portions comprise at least one communication channel portion extending across
4 each of the opposing surfaces of the substrate.

5
6 **37. (New)** A memory module as recited in claim 34, wherein each
7 communication channel portion comprises a plurality of conductors that follow a
8 substantially linear path across the substrate.

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10 **38. (New)** A memory module as recited in claim 34, wherein each
11 communication channel portion comprises a plurality of conductors having lengths
12 that are approximately equal.

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